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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/549,291	09/14/2005	Junko Iwanaga	071971-0361	8090

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EXAMINER	
LIN, JOHN	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/549,291	IWANAGA ET AL.	
	Examiner	Art Unit	
	John Lin	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *9-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *16 September 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 9-11 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on May 23, 2007.

2. Applicant's election without traverse of claims 1-8 in the reply filed on May 23, 2007 is acknowledged.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a) because they fail to show the semiconductor FIN having a convex shape as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each

drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 6 recites the limitation "the gate insulating film." There is insufficient antecedent basis for this limitation in the claim. For the purpose of applying art, it will be interpreted as the first gate insulating film.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Shirasaki (US 4,996,574).

Claim 1: Shirasaki teaches a semiconductor device (Figs. 10 and 10A) comprising:

a semiconductor substrate (32) in which a trench (30) is formed;

a source region (31a) and a drain region (31b), each of which is buried in the trench and contains an impurity of the same conductive type;

a semiconductor FIN (31c) buried in the trench and provided between the source region and the drain region;

a gate insulating film (34) provided on a side surface of the semiconductor FIN as well as an upper surface of the semiconductor FIN; and

a gate electrode (35) having two end portions (portions in the trenches) each of which protrudes downward in the trench so as to extend along the gate insulating film on the semiconductor FIN and formed on the gate insulating film (column 7, lines 35-67).

Claim 2: Shirasaki teaches the semiconductor FIN is made of silicon (column 7, lines 40-45).

Claim 4: Shirasaki teaches the gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate,

wherein the gate insulating film is provided on the side and upper surfaces of the semiconductor FIN as well as part of the semiconductor substrate in which the trench is not formed, and

wherein part of the gate insulating film located on the part of the semiconductor substrate in which the trench is not formed is interposed between the semiconductor substrate and the gate electrode (Figs. 10 and 10A).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shirasaki in view of Hayashi et al. (US 4,868,632).

Claim 3: Shirasaki teaches all the limitations of claim 1 and further teaches the gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate (Figs. 10 and 10A), but do not teach an isolation insulating film is further provided between part of the semiconductor substrate located in a side wall portion of the trench and part of the gate electrode located over the side wall of the semiconductor FIN and an insulating film is further provided between part of the semiconductor substrate in which the trench is not formed and the gate electrode. However, Hayashi et al. teach a gate insulating film with three layers (106, 017, 108; Fig. 1; column 3, lines 15-28). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have made the gate insulating layer of Shirasaki three layers as taught by Hayashi et al. to have better insulated the gate from the rest of the transistor.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shirasaki in view of Yang et al. (US 6,787,854).

Claim 5: Shirasaki teaches all the limitations of claim 1, but do not teach the semiconductor FIN is formed so as to have a convex shape when viewed from the bottom of the trench. However, Yang et al. teach a convex shaped fin structure that improves device performance (column 2, lines 32-41). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have made the semiconductor FIN of Shirasaki have a convex shape as taught by Yang et al. in order to improve device performance.

10. Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shirasaki and Lee et al. (6,025,628) in view of Abadeer et al. (7,163,851).

Claim 6: Shirasaki teaches a field-effect transistor (Figs. 10 and 10A) including a semiconductor substrate (32) in which a trench (30) is formed, a source region (31a) and a drain region (31b) each of which is buried in the trench and contains an impurity of the same conductive type, a semiconductor FIN (31c) buried in the trench and provided between the source region and the drain region, a gate insulating film (34) provided on a side surface of the semiconductor FIN as well as an upper surface of the semiconductor FIN, and a gate electrode having two end portions each of which protrudes downward in the trench so as to extend along the gate insulating film on the semiconductor FIN and formed on the gate insulating film (column 7, lines 35-67).

Lee et al. teach a field-effect transistor (Fig. 1B) including a gate insulating film (20) provided on a semiconductor substrate (12), a gate electrode (39) provided on the gate insulating film, and source (24) and drain (26) regions each of which contains an

impurity and is provided in a region of the semiconductor substrate located on a side of and under the gate electrode (column 4, lines 7-63).

But Shirasaki and Lee et al. do not teach two field-effect transistors on the same substrate. However Abadeer et al. teach a FinFet integrated with another FET in order increase device density (columns 1 and 2, lines 7-67 and 1-4 respectively). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have integrated the field-effect transistor of Shirasaki and the field-effect transistor of Lee et al. on the same substrate in order to increase device density.

Claim 8: Shirasaki teaches the gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate,

wherein the gate insulating film is provided on the side and upper surfaces of the semiconductor FIN as well as part of the semiconductor substrate in which the trench is not formed, and

wherein part of the gate insulating film located on the part of the semiconductor substrate in which the trench is not formed is interposed between the semiconductor substrate and the gate electrode (Figs 10 and 10A).

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shirasaki and Lee et al. in view of Abadeer et al. as applied to claims 6 and 8 above, and further in view of Hayashi et al

Claim 7: Shirasaki teaches all the limitations of claim 6 and further teaches the gate electrode is provided on the gate insulating film so as to extend over the

semiconductor substrate (Figs. 10 and 10A), but do not teach an isolation insulating film is further provided between part of the semiconductor substrate located in a side wall portion of the trench and part of the gate electrode provided over the side surface of the semiconductor FIN and an insulating film is further provided between part of the semiconductor substrate and the gate electrode. However, Hayashi et al. teach a gate insulating film with three layers (106, 017, 108; Fig. 1; column 3, lines 15-28). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have made the gate insulating layer of Shirasaki three layers as taught by Hayashi et al. to have better insulated the gate from the rest of the transistor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Lin whose telephone number is 571-270-1274. The examiner can normally be reached on M-Th 8:00-5:30EST F-8:30-5:00EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John Lin

EUGENE LEE
PRIMARY EXAMINER